

FIG. 1

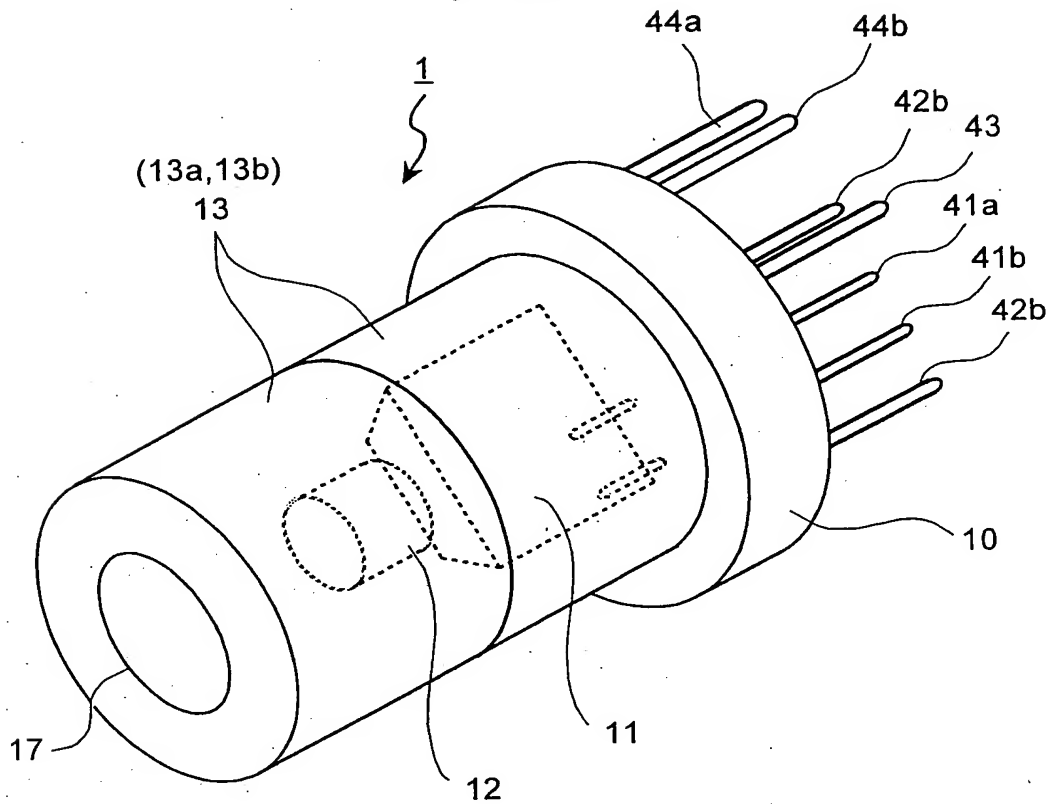
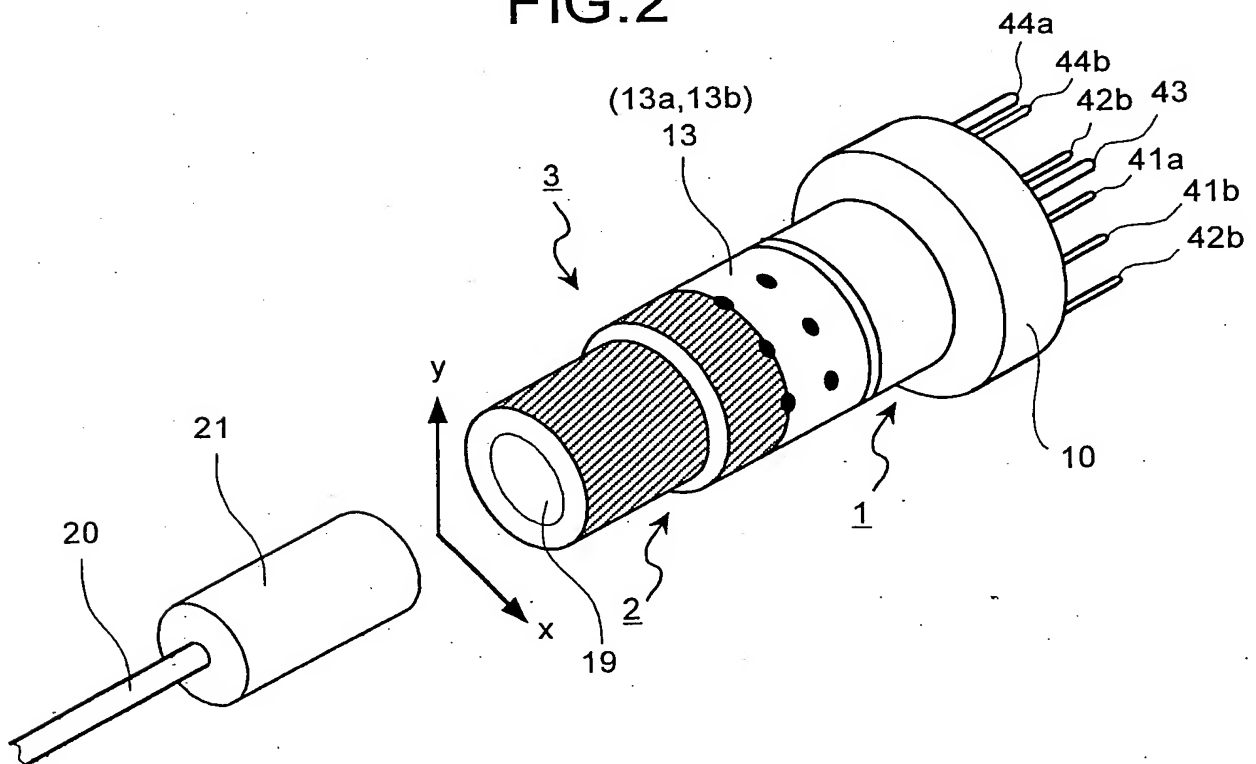


FIG. 2



**FIG. 3A**

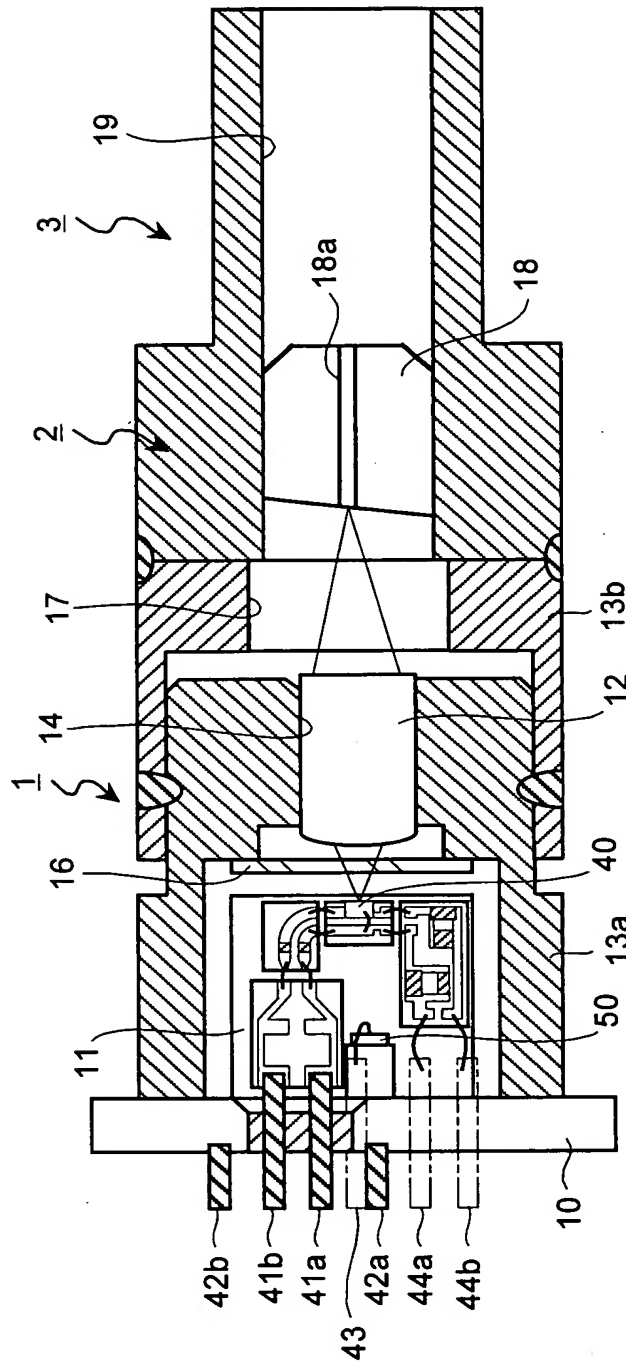
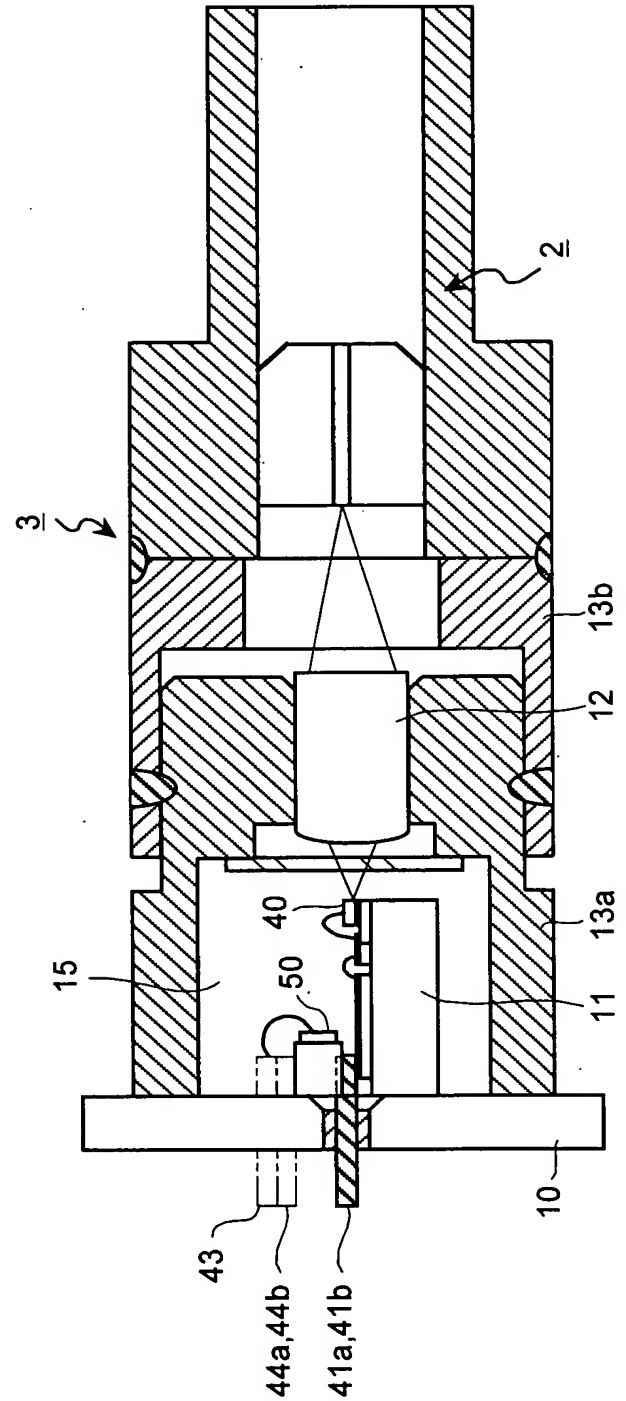


FIG. 3B



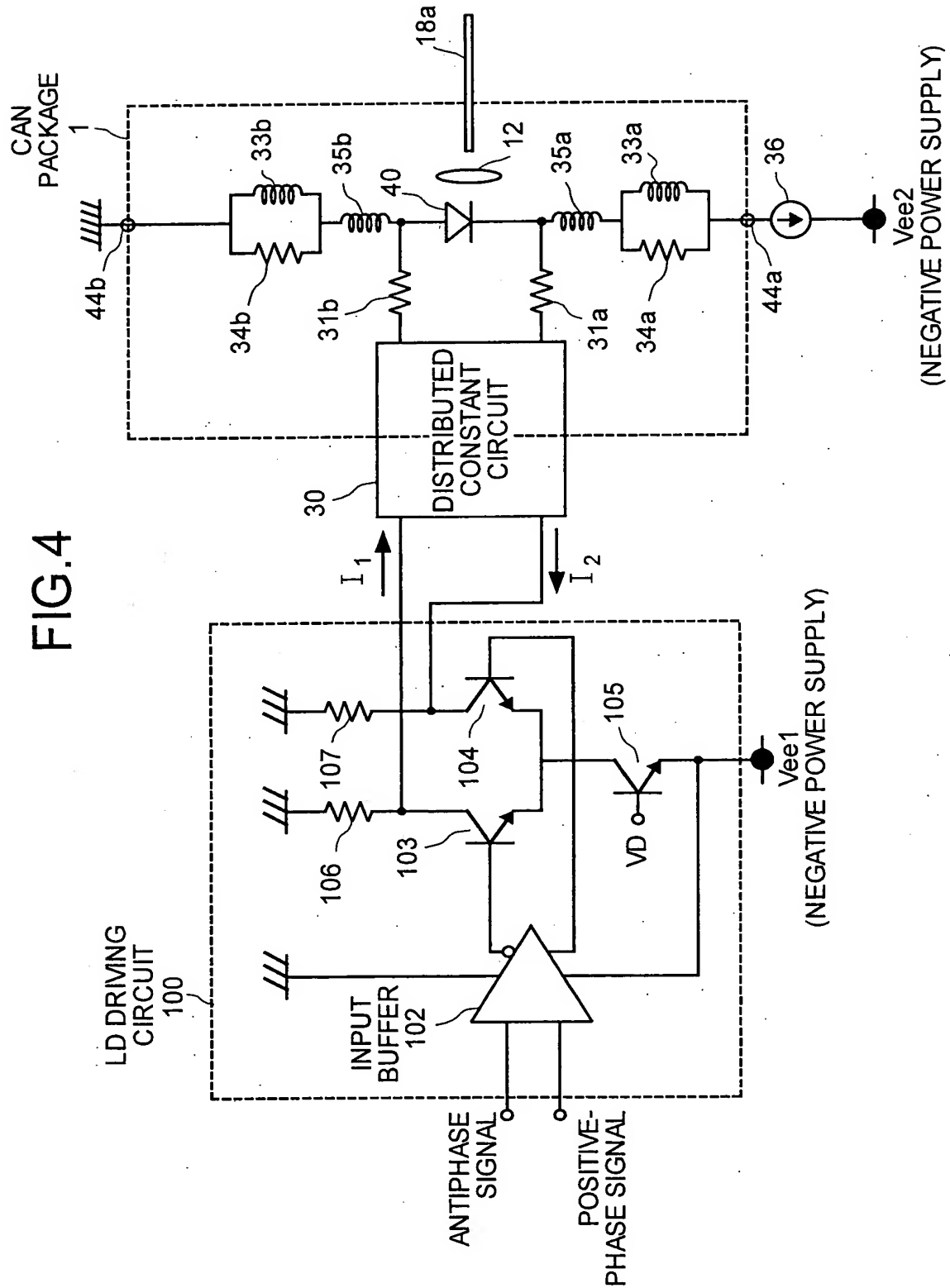


FIG. 5

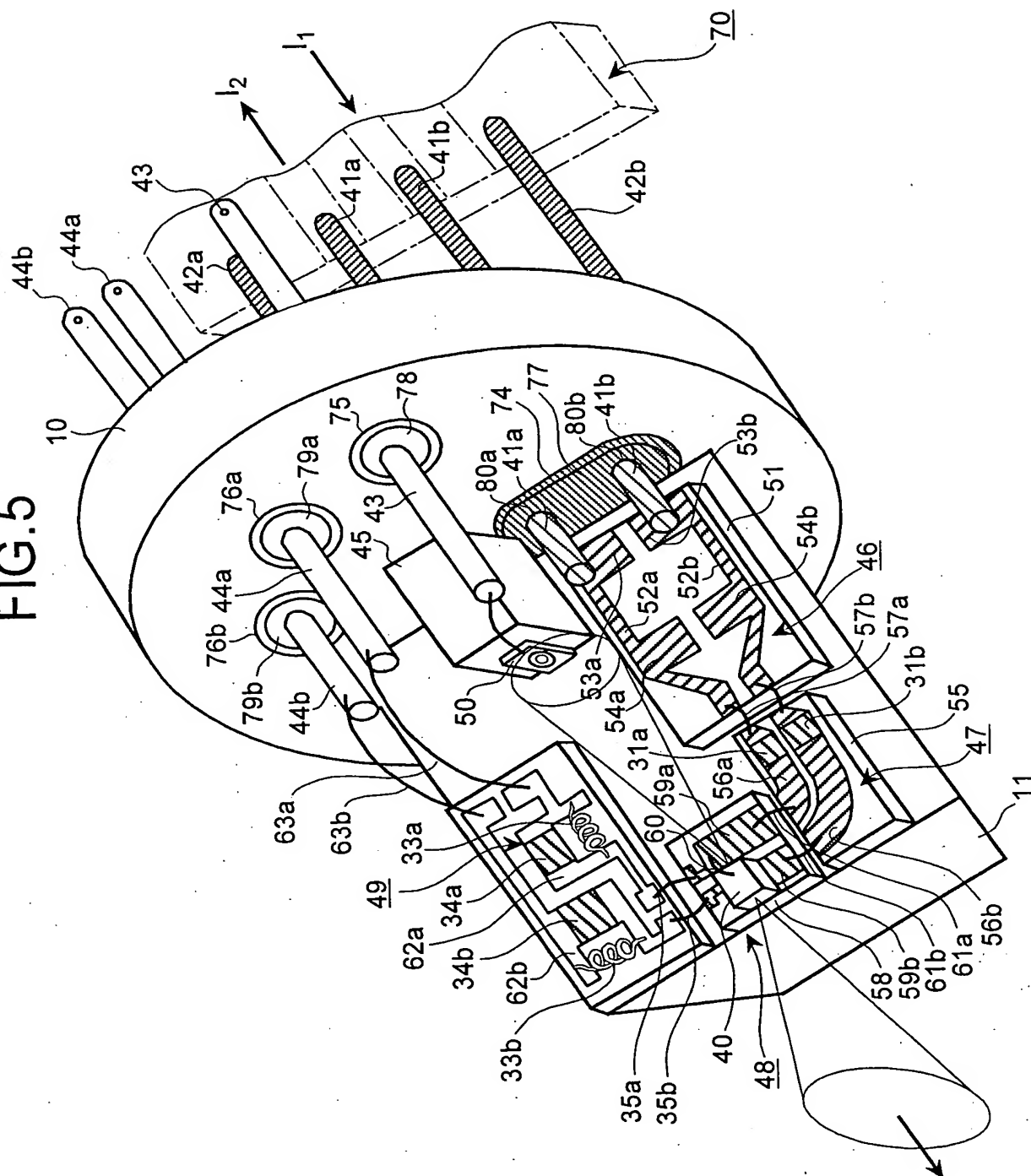






FIG.8

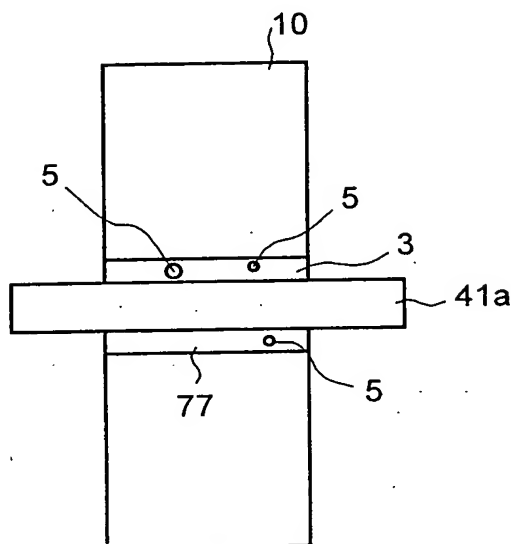


FIG.9

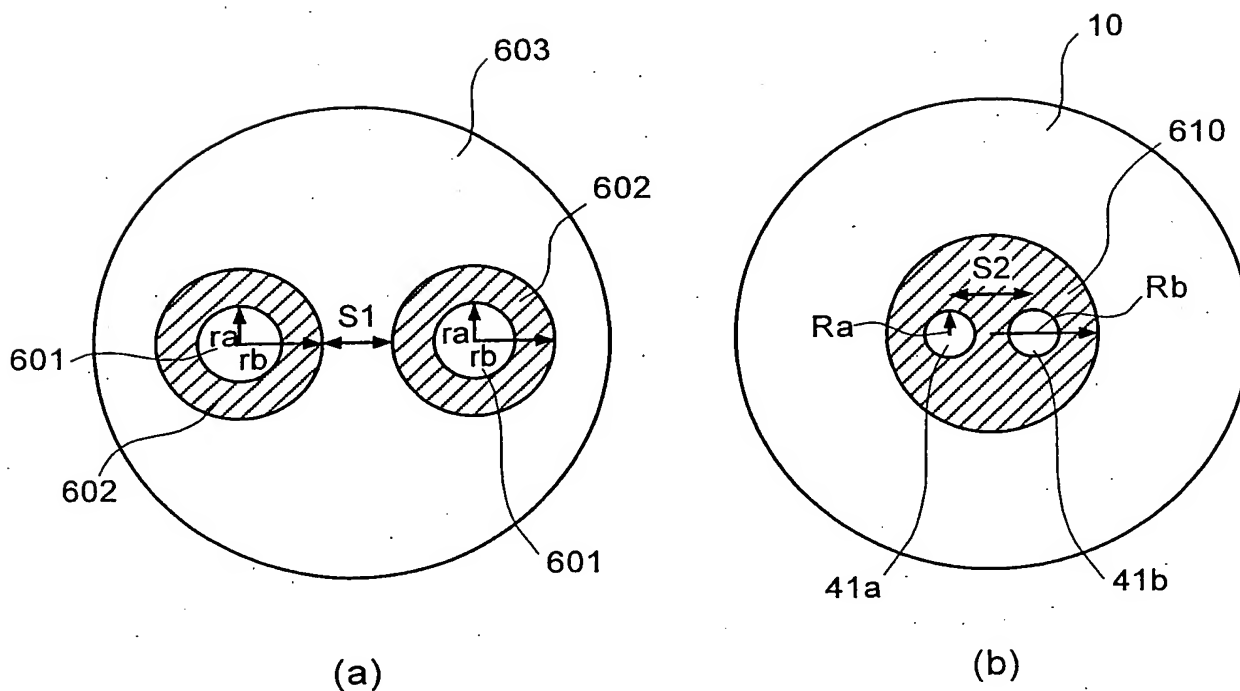


FIG.10A

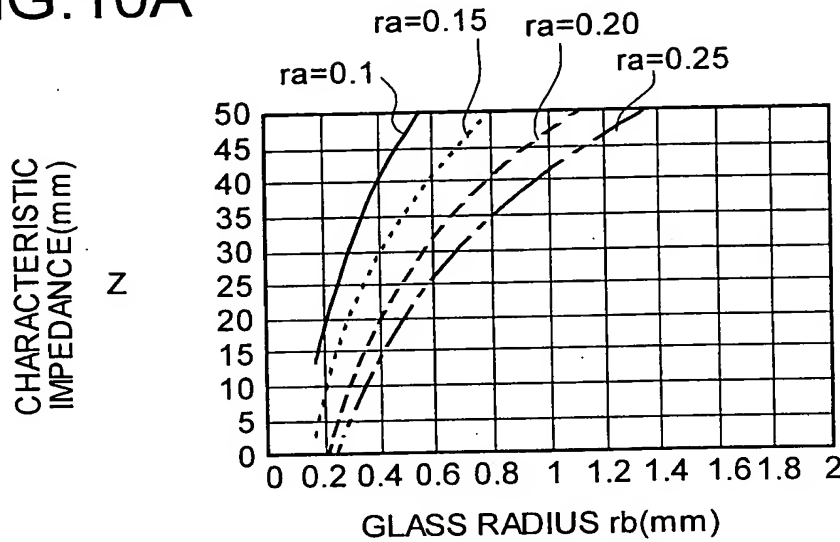


FIG.10B

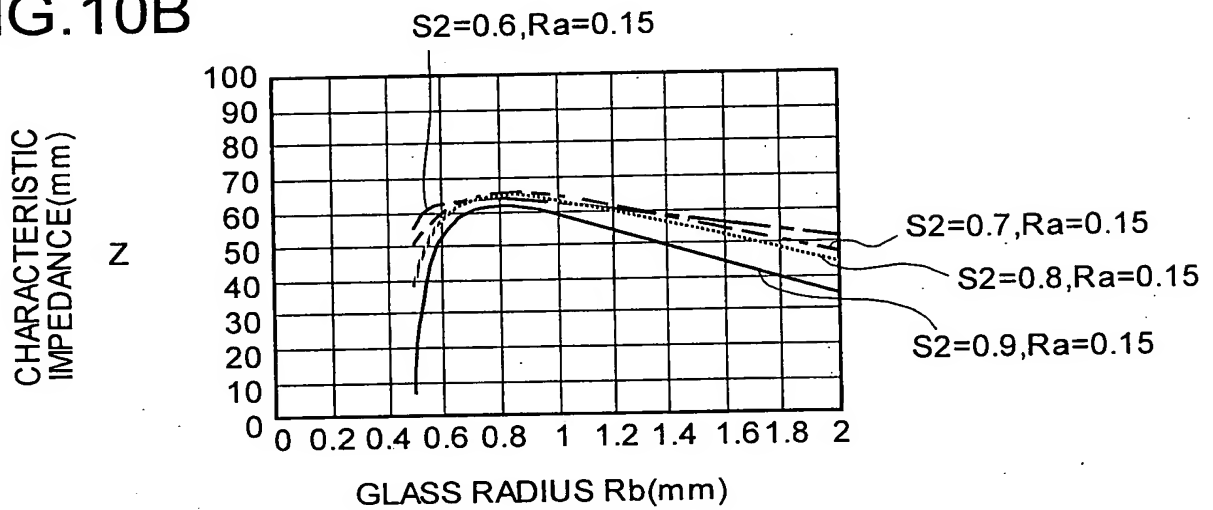


FIG.10C

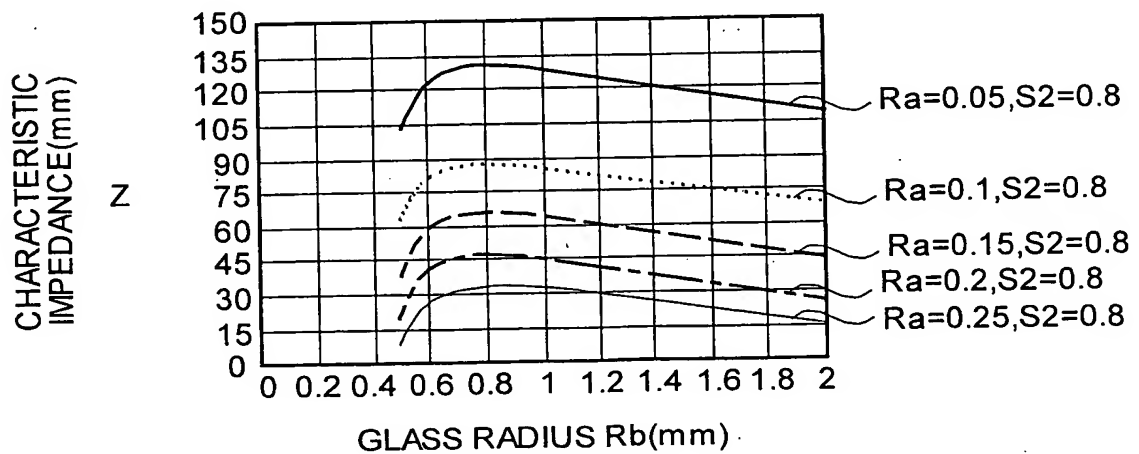




FIG. 11

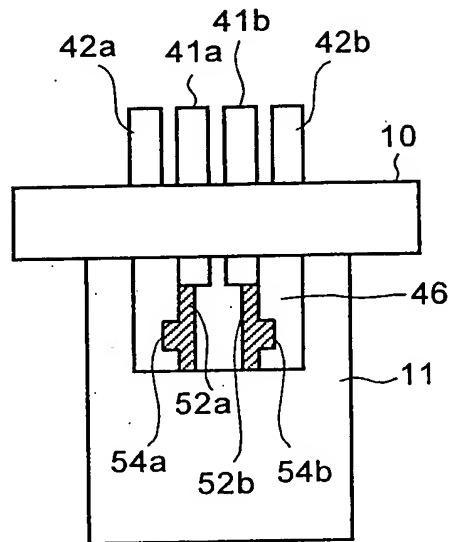


FIG. 12

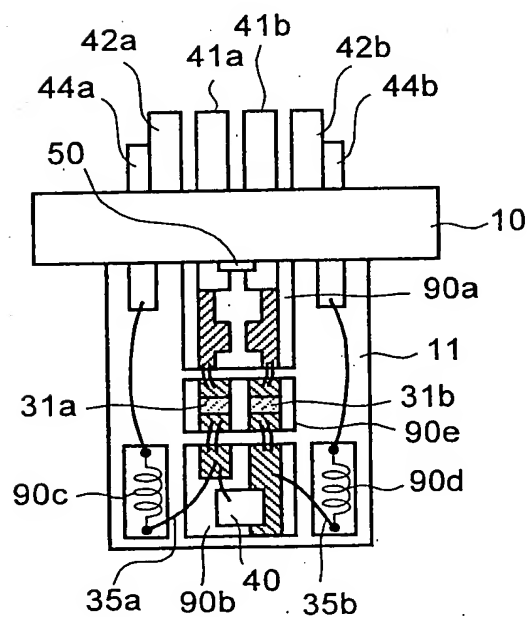


FIG. 13

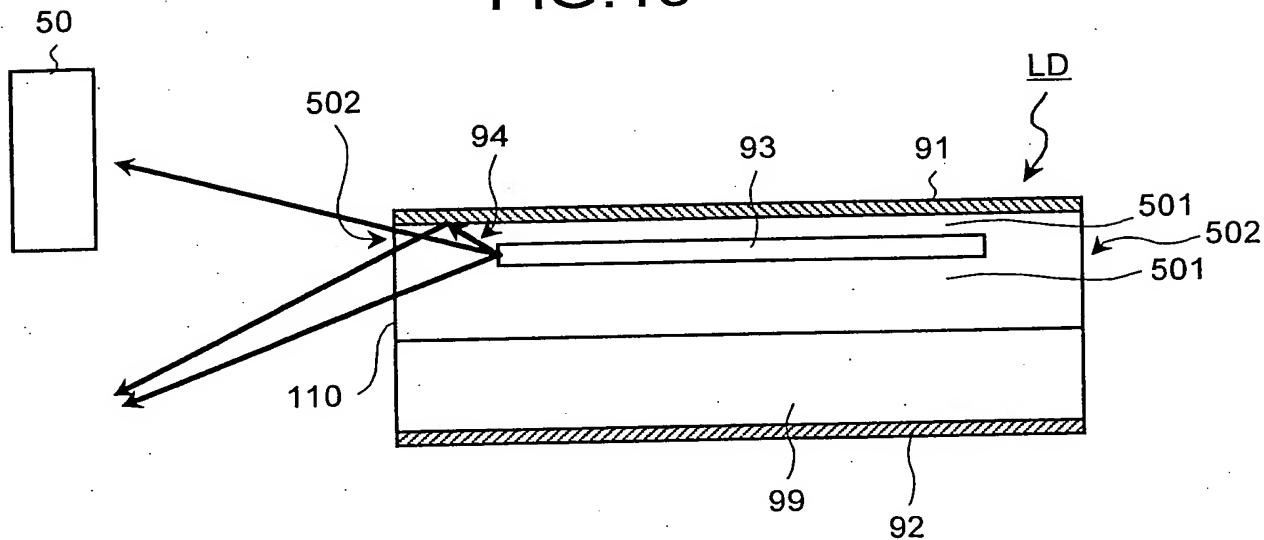
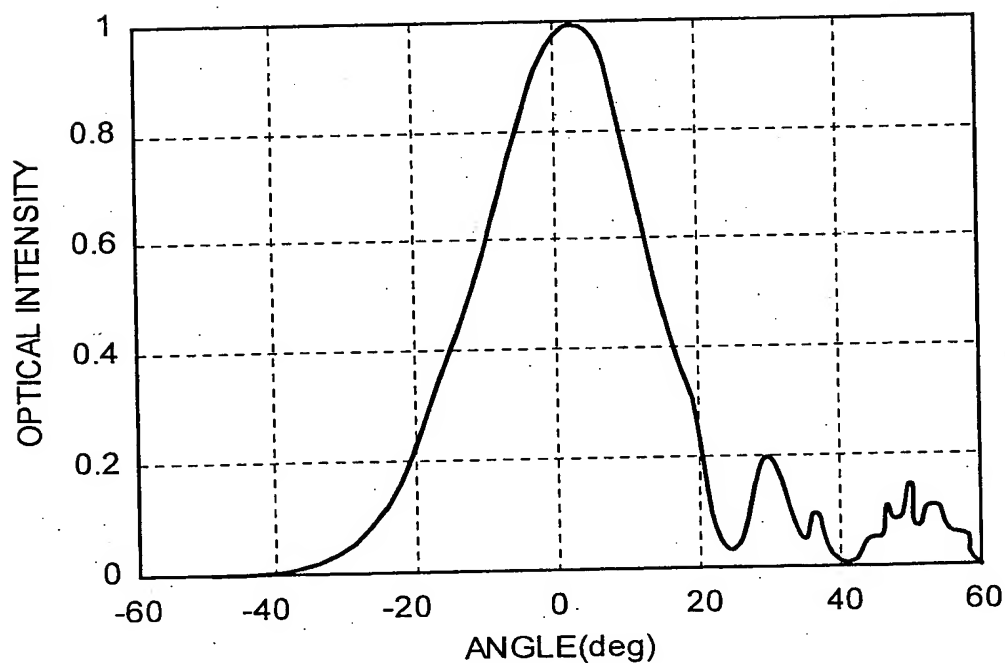


FIG. 14



→ SEMICONDUCTOR SUBSTRATE SIDE

FIG. 15

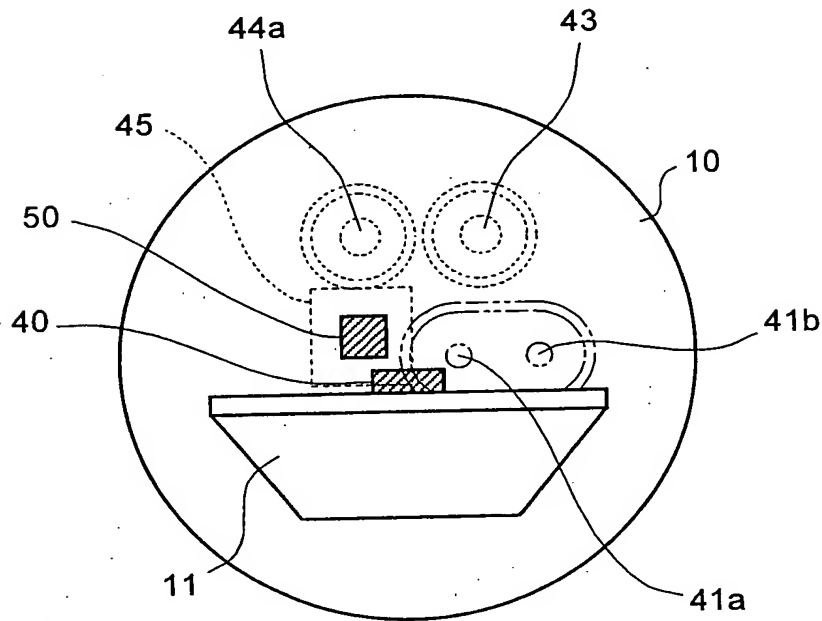


FIG. 16

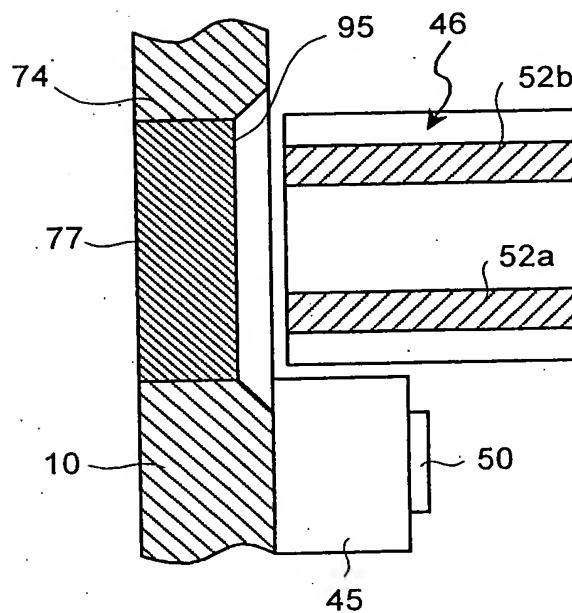


FIG. 17

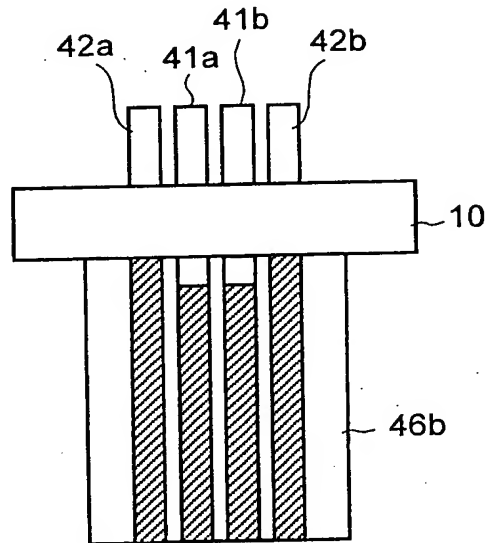
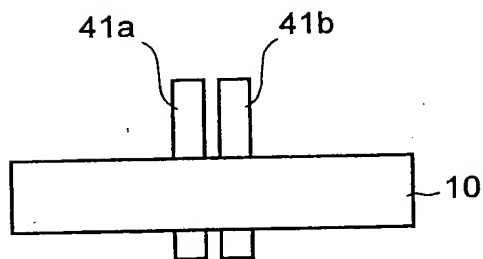


FIG. 18



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FIG.19A

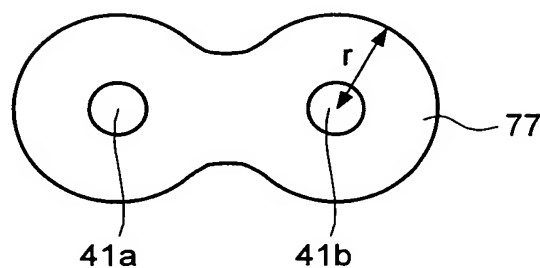


FIG.19B

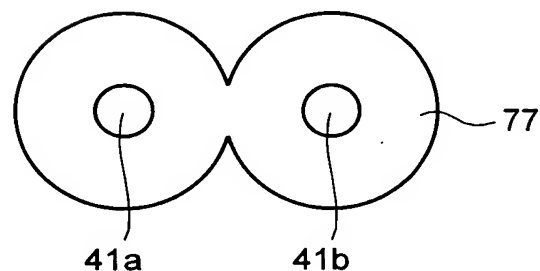


FIG.19C

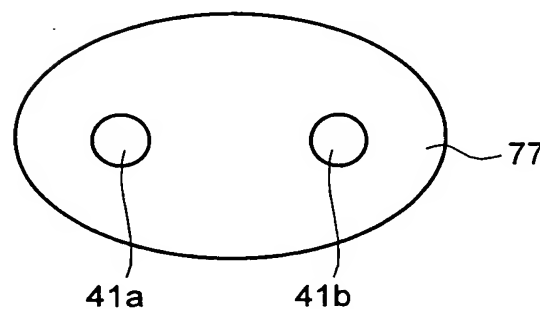
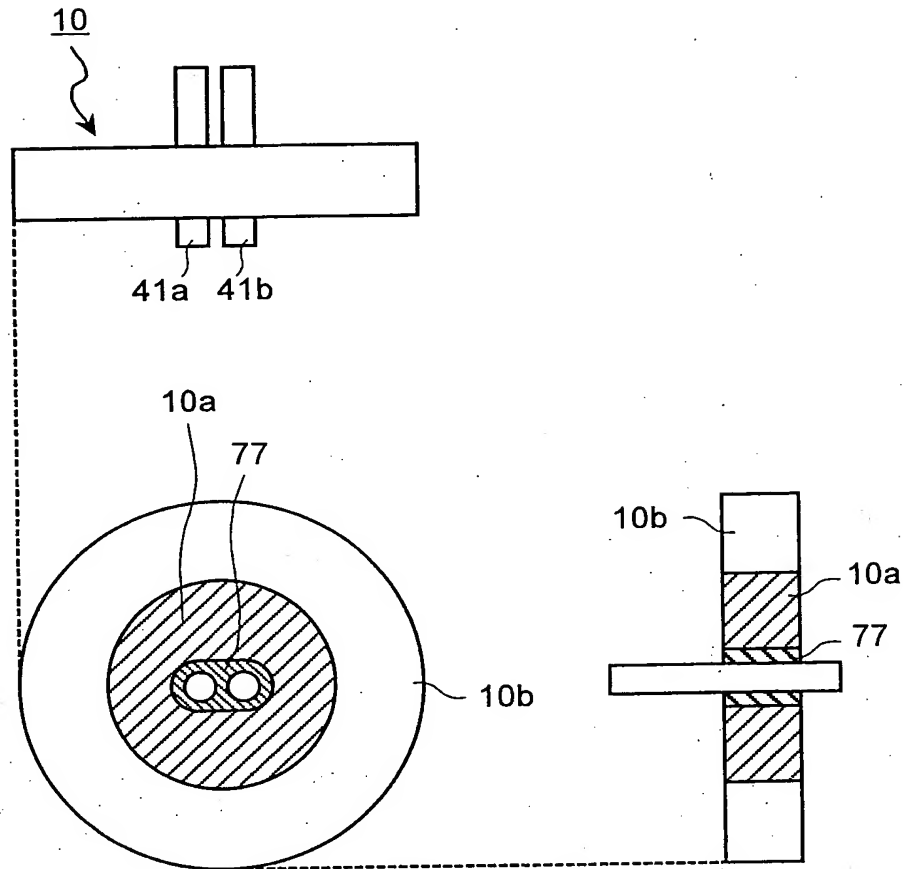


FIG. 20



**FIG.21B**

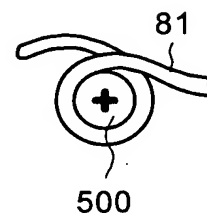


FIG. 22

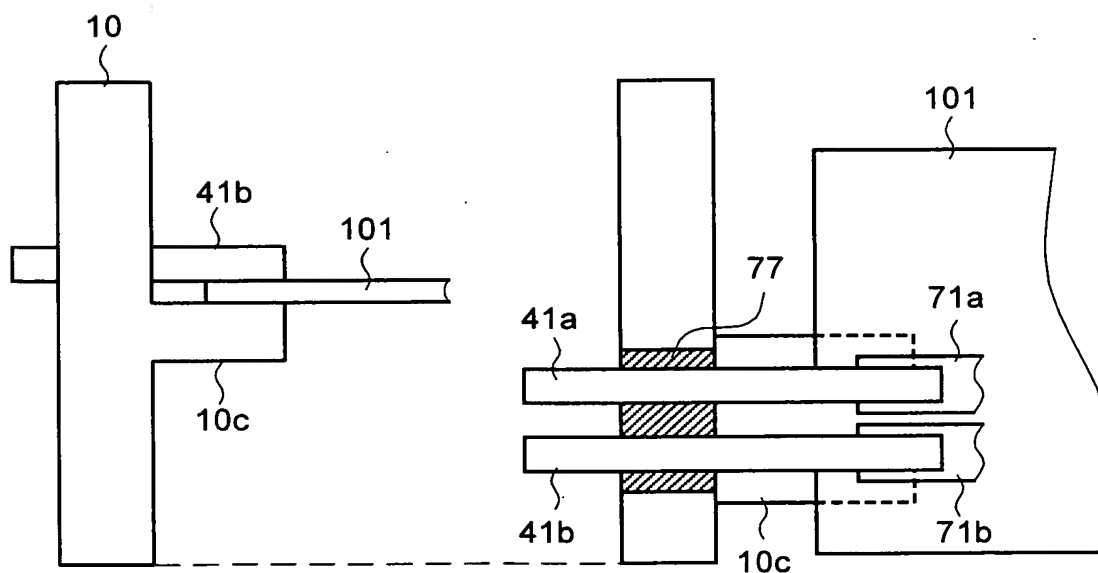
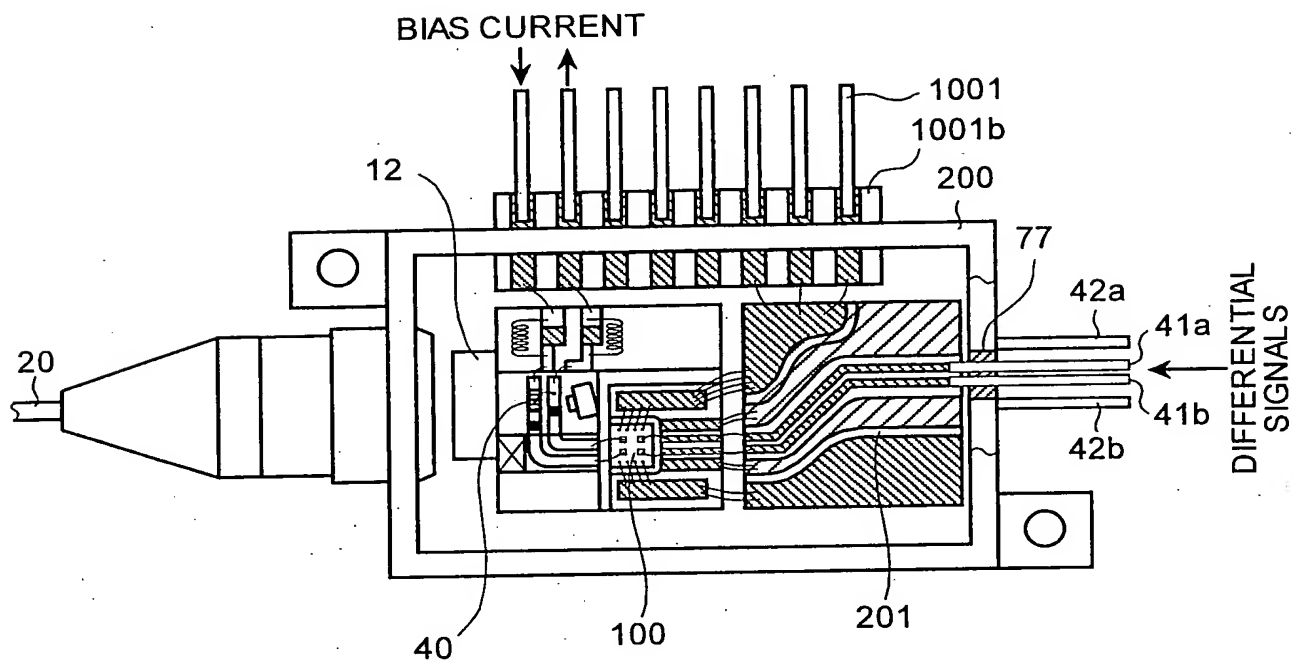
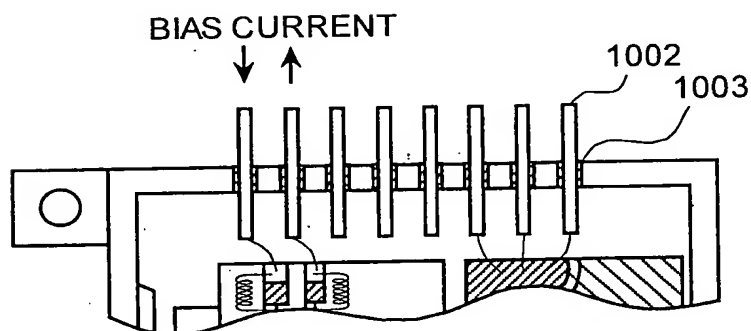


FIG.23



(a)



(b)